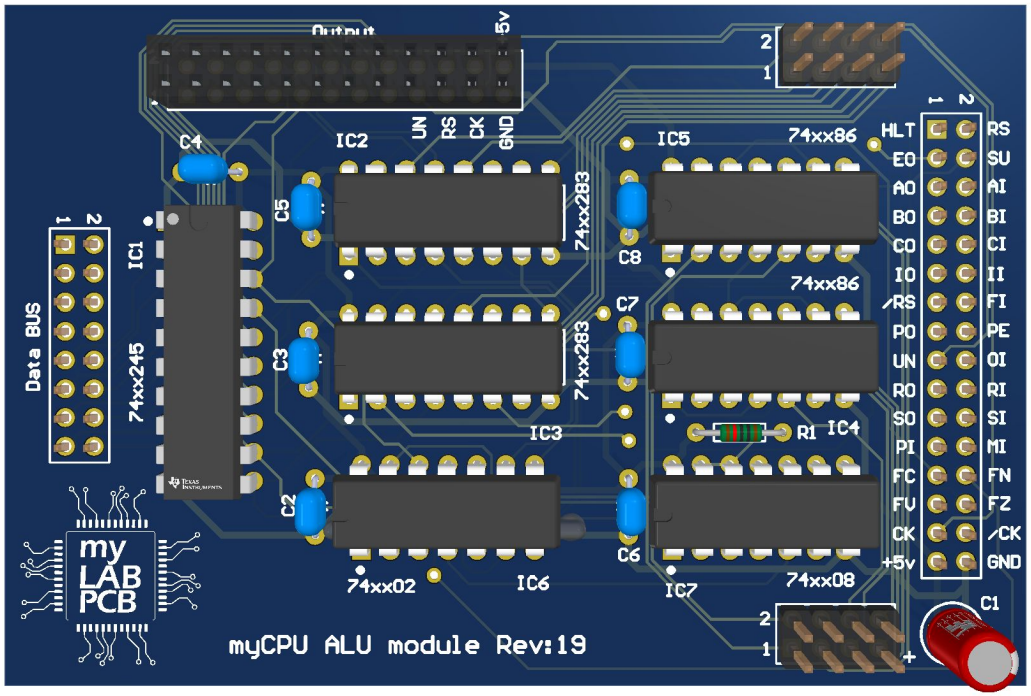
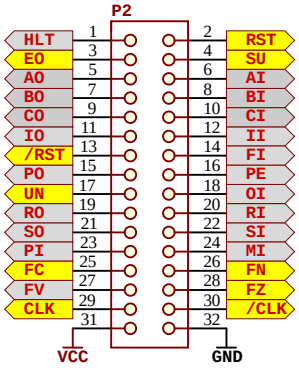
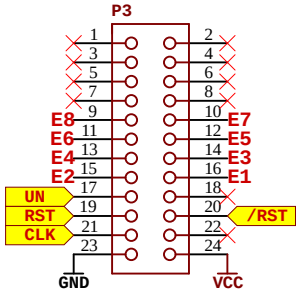

Output
5v
UN
RS
CK
GND
2
1
1
2
C4
IC2
74xx283
C5
IC5
74xx86
C8
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
Data BUS
IC1
74xx245
C3
C7
74xx283
74xx86
IC3
R1
IC4
C2
C6
74xx02
IC6
IC7
74xx08
C1
my
LAB
PCB
myCPU ALU module Rev:19

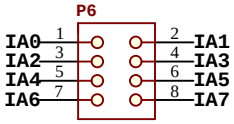
Control BUS Connector



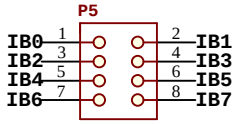
OUTPUT Connector



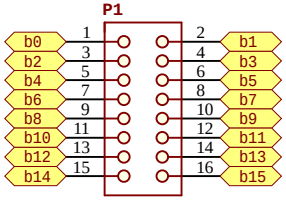
Register A input



Register B Input

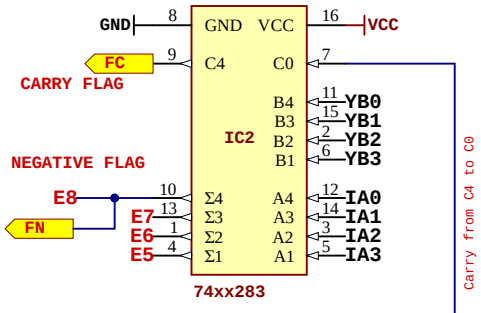


Data BUS Connector

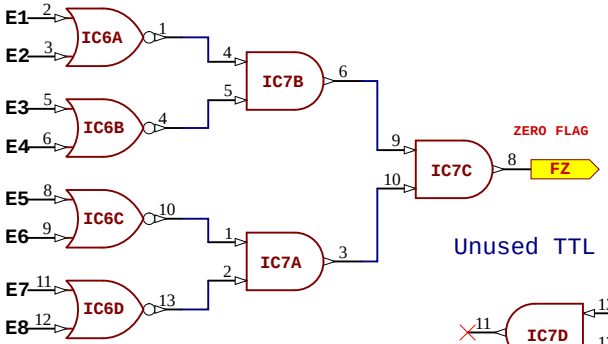


Input significative bit weigh goes from IA7 or YB7 (lower) to IA0 or YB0 (higher)

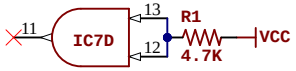
Operation goes from E1 to E4 and carry is passed from C4 to C0.
The ADDER inputs order goes from A1,B1 to A4,B4
Cascade is from IC3 to IC2.

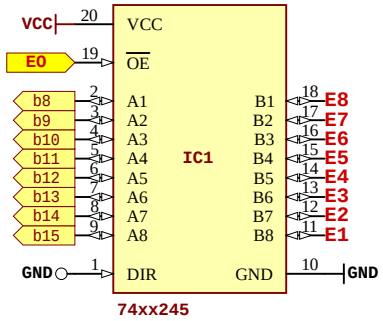


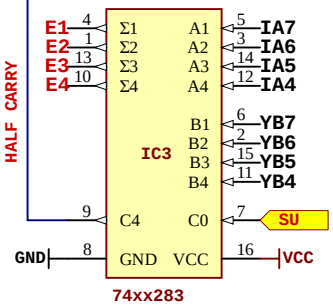
Zero Flag Logic

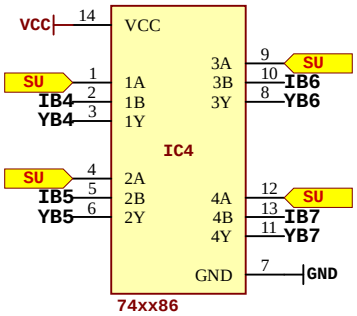


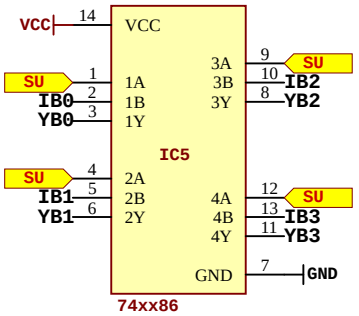
Unused TTL Inputs

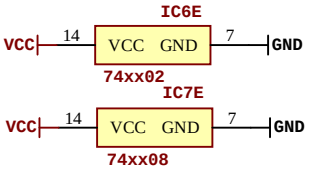


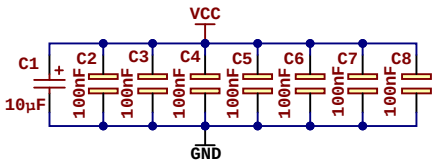












Decoupling Capacitors

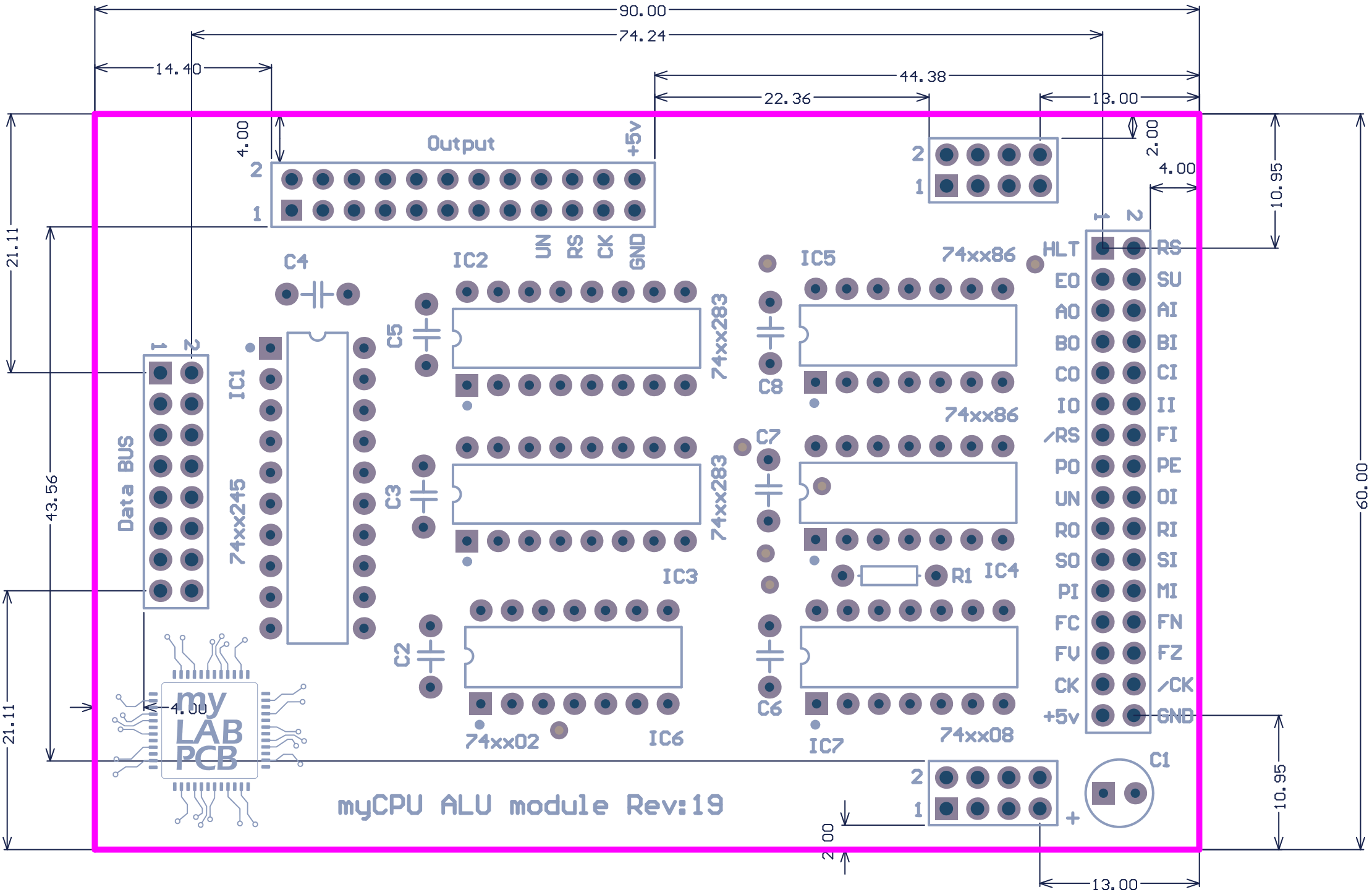
CO pin, initial carry should set to SU signal. On ADD operation SU is LOW and Carry is 0, for SUB operation SU is HIGH and Carry becames 1 to accomplish two'complement binary representation.

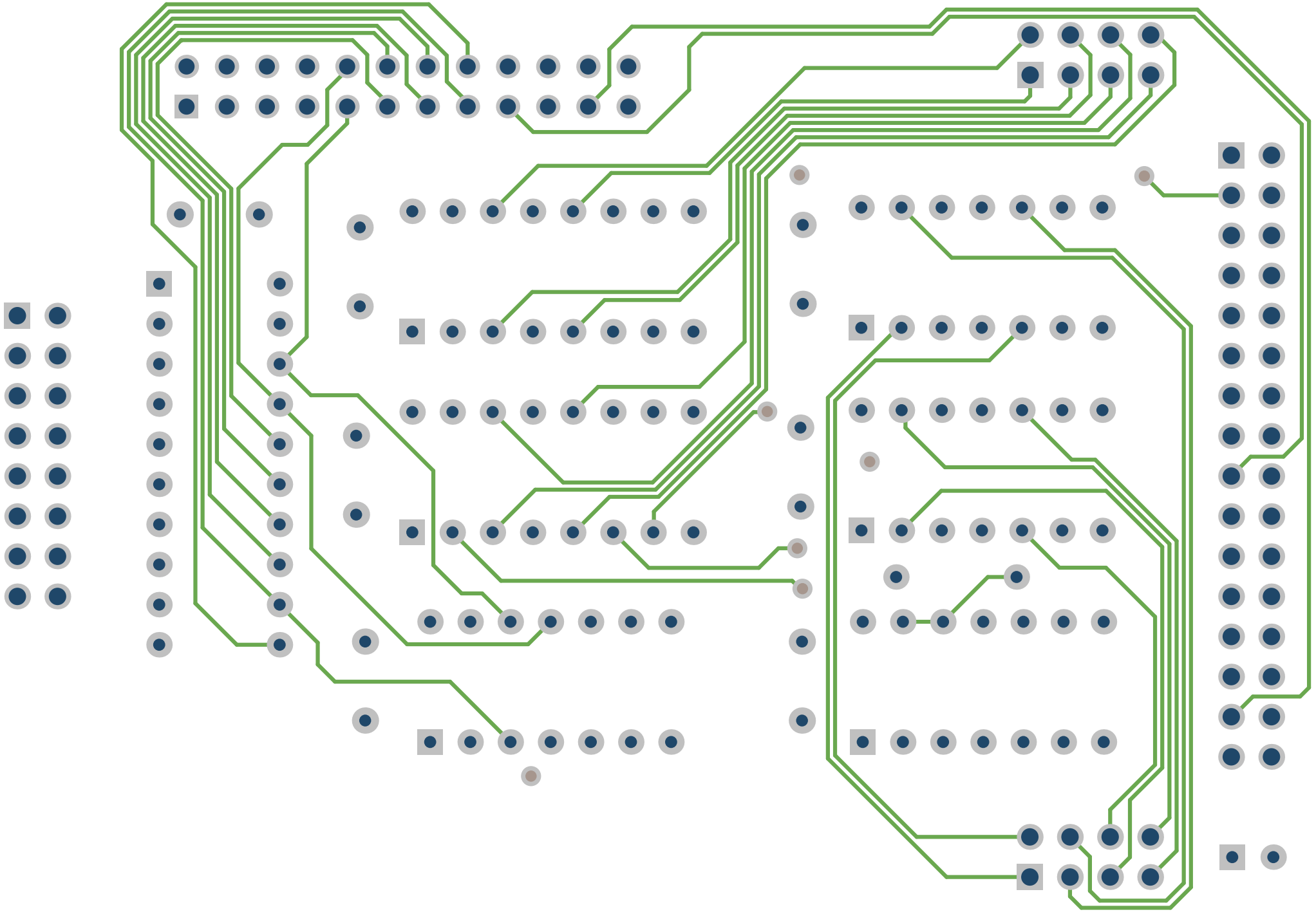
my LAB PCB

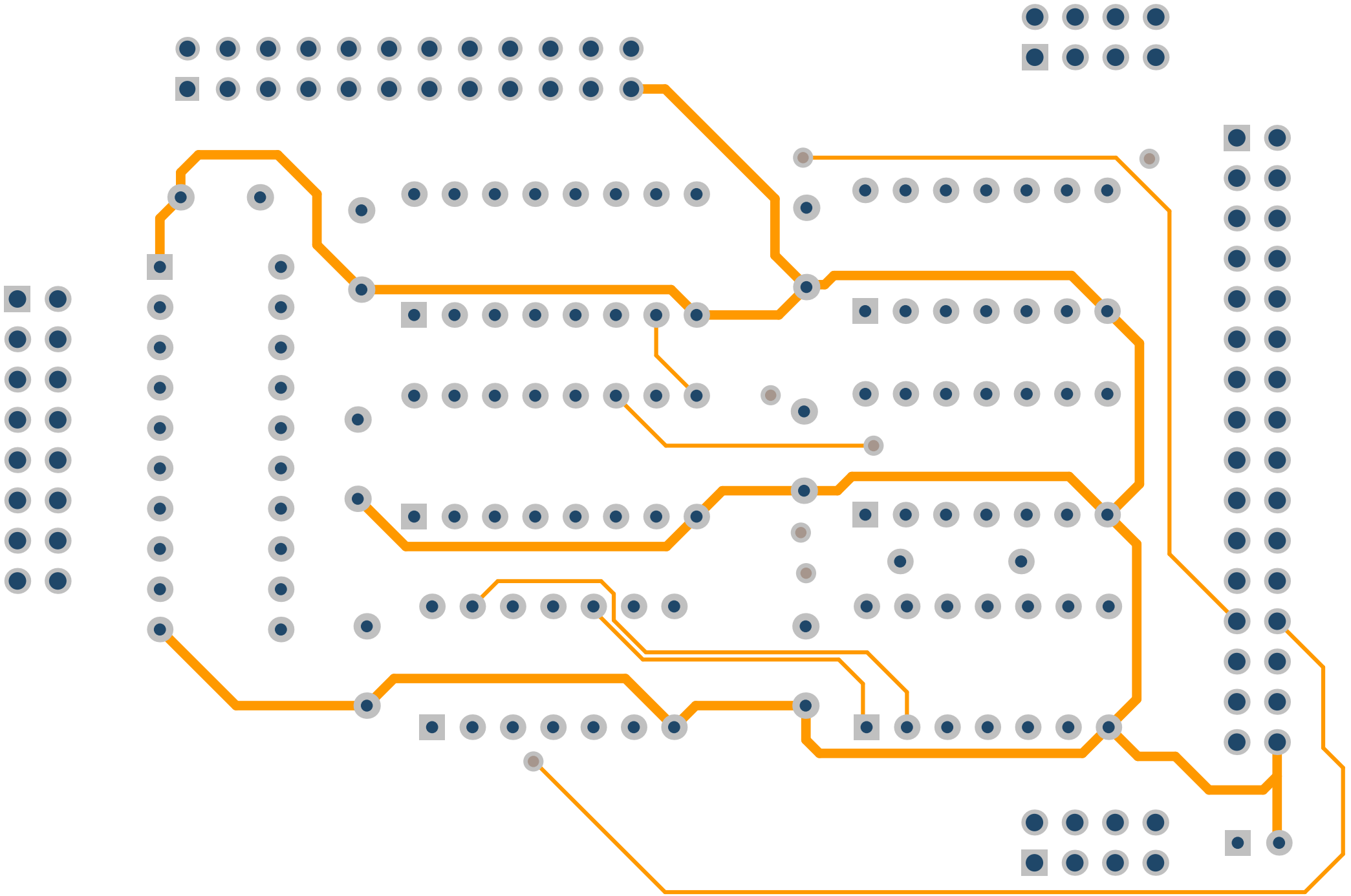
Project: myCPU ALU module

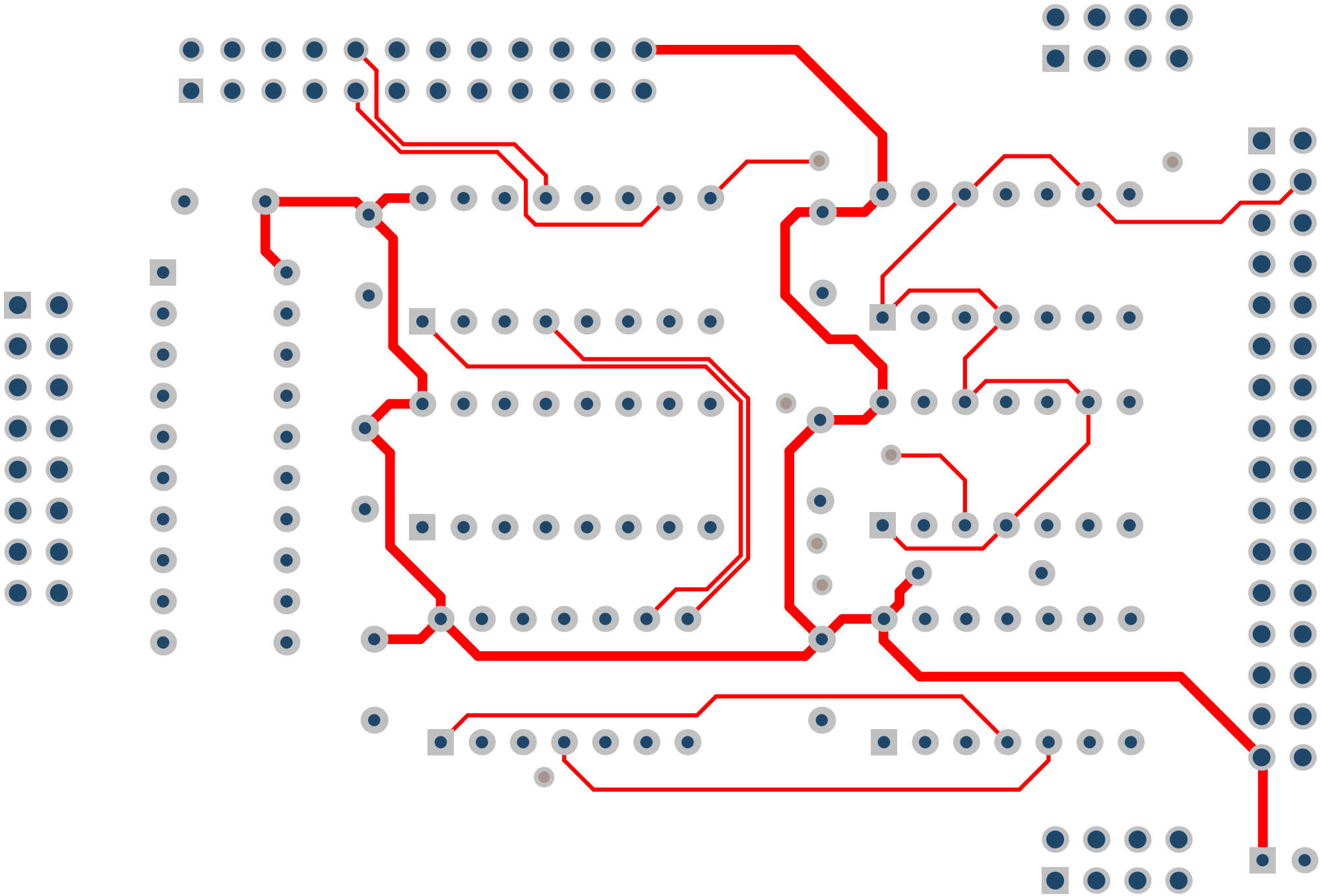
Revision: 19 **Date:** 06-Apr-24

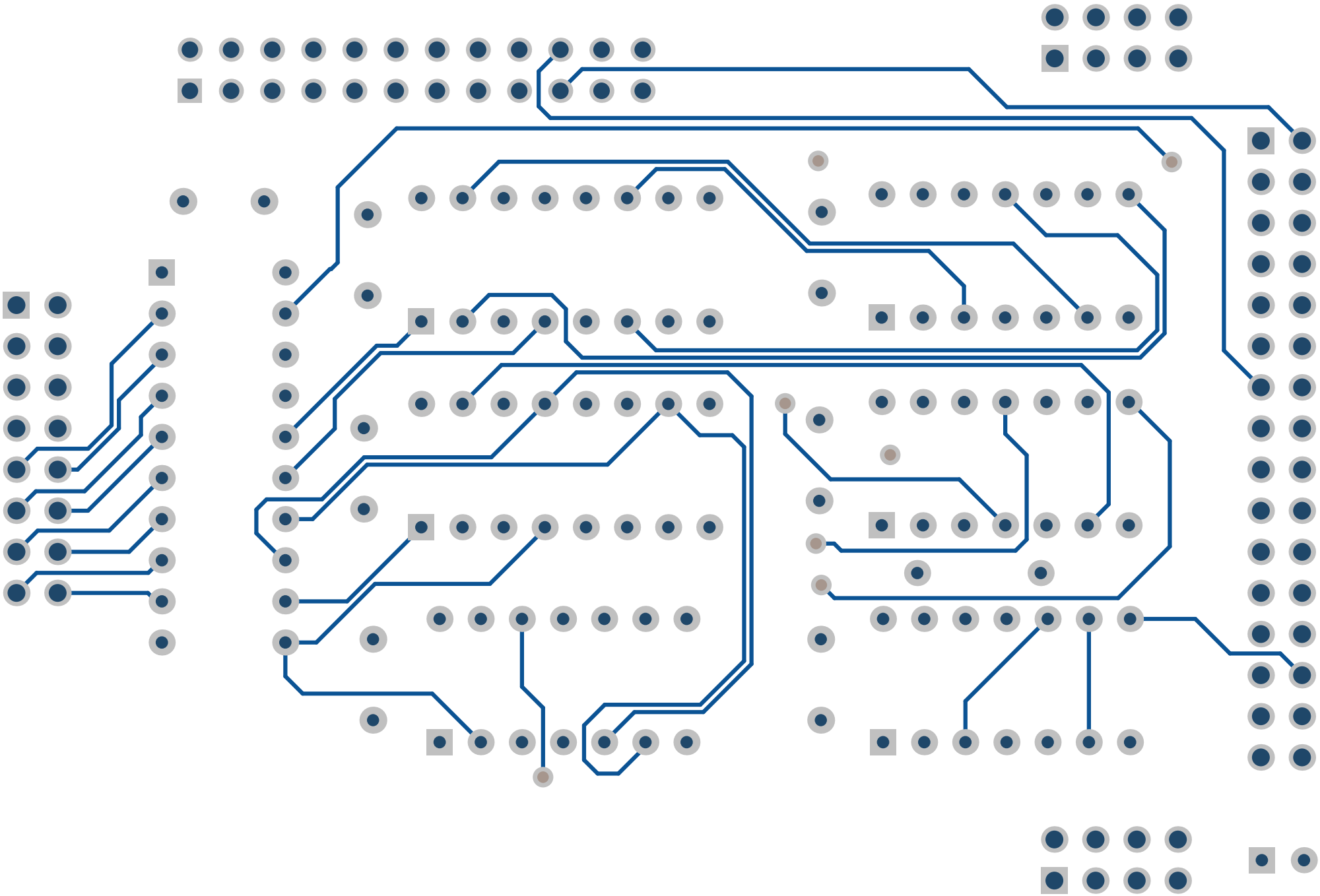
Author: Rafa Hernández


90.00
74.24
14.40
44.38
22.36
13.00
4.00
2.00
21.11
43.56
10.95
60.00
Output
+5v
UN
RS
CK
GND
C4
IC2
74xx283
C5
C3
C2
IC1
74xx245
Data BUS
IC3
IC6
74xx02
C8
IC5
74xx86
C7
R1
IC4
C6
IC7
74xx08
C1
HLT
EO
AO
BO
CO
IO
/RS
PO
UN
RO
SO
PI
FC
FV
CK
+5v
RS
SU
AI
BI
CI
II
FI
PE
OI
RI
SI
MI
FN
FZ
/CK
GND
myCPU ALU module Rev:19









Bill of Materials

myCPU ALU module

Description	Value	Q
Electrolytic capacitor 16v/50v	10µF	1
Ceramic capacitor	100nF	7
Non inverting bus transceiver	74xx245	1
4-Bits Full adder with fast carry	74xx283	2
Quad 2-input XOR gates	74xx86	2
Quad 2-input NOR gates	74xx02	1
Quad 2-input AND gates	74xx08	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p	1
Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p	1
Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	8p	2
Resistor Axial	4.7K	1

Assembly List

myCPU ALU module

Designator	Description	Value
C1	Electrolytic capacitor 16v/50v	10µF
C2	Ceramic capacitor	100nF
C3	Ceramic capacitor	100nF
C4	Ceramic capacitor	100nF
C5	Ceramic capacitor	100nF
C6	Ceramic capacitor	100nF
C7	Ceramic capacitor	100nF
C8	Ceramic capacitor	100nF
IC1	Non inverting bus transceiver	74xx245
IC2	4-Bits Full adder with fast carry	74xx283
IC3	4-Bits Full adder with fast carry	74xx283
IC4	Quad 2-input XOR gates	74xx86
IC5	Quad 2-input XOR gates	74xx86
IC6	Quad 2-input NOR gates	74xx02
IC7	Quad 2-input AND gates	74xx08
P1	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	16p
P2	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	32p
P3	Socket Header, THT, pitch 2.54mm, Dual Row, Vertical	24p
P5	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	8p
P6	Pin Header, THT, pitch 2.54mm, Dual Row, Vertical	8p
R1	Resistor Axial	4.7K